

CLAIMS

- 1 1. A method of forming a semiconductor substrate, comprising:
2 providing a structure comprising a first layer having a first oxidation rate disposed over a
3 second layer having a second oxidation rate, wherein the first oxidation rate is greater than the
4 second oxidation rate;
5 reacting said first layer to form a sacrificial layer; and
6 removing said sacrificial layer to expose said second layer.
- 1 2. The method as claimed in claim 1, wherein the second layer comprises a strained
2 semiconductor.
- 1 3. The method as claimed in claim 1, wherein the second layer comprises Si.
- 1 4. The method as claimed in claim 1, wherein the first layer comprises Si or Ge.
- 1 5. The method as claimed in claim 1, wherein said semiconductor substrate further
2 comprises a relaxed semiconductor layer disposed beneath said second layer.
- 1 6. The method as claimed in claim 5, wherein said relaxed semiconductor layer comprises Si
2 or Ge.

1 7. The method as claimed in claim 1, wherein said semiconductor substrate further
2 comprises an insulator layer disposed beneath said second layer.

1 8. The method as claimed in claim 7, wherein said insulator layer comprises silicon dioxide.

1 9. The method as claimed in claim 1, wherein said step of reacting said first layer to form a
2 sacrificial layer comprises thermal oxidation.

1 10. The method as claimed in claim 9, wherein said thermal oxidation is performed at or
2 below a temperature of approximately 850°C.

1 11. The method as claimed in claim 9, wherein said thermal oxidation is performed at a
2 temperature at or below approximately 700°C.

1 12. The method as claimed in claim 1, wherein said step of reacting said first layer to form a
2 sacrificial layer comprises chemical oxidation.

1 13. The method as claimed in claim 1, wherein said step of reacting said first layer to form a
2 sacrificial layer is performed on a first region of said first layer and not on a second region of said
3 first layer.

1 14. The method as claimed in claim 13, wherein said method further comprises forming a
2 surface channel device in said first region.

1 15. The method as claimed in claim 13, wherein said method further comprises forming a
2 buried channel device in said second region.

1 16. The method as claimed in claim 13, wherein said method further comprises:
2 forming a surface channel device in said first region; and
3 forming a buried channel device in said second region, wherein the channel of said
4 surface channel device and said buried channel device comprises a second device layer.

1 17. The method as claimed in claim 16, wherein said second layer comprises Si and said first
2 layer comprises SiGe.

1 18. The structure formed by the method of claim 1.

1 19. The structure formed by the method of claim 7.

1 20. The structure formed by the method of claim 16.

1 21. A method of forming devices on a substrate said method comprising the steps of:

providing a structure comprising a SiGe layer disposed over a strained semiconductor layer;

selectively removing said SiGe layer in a first region but not in a second region such that a surface channel device may be formed on said first region and a buried channel device may be formed on said second region.

22. A method of forming devices on a substrate, said method comprising the steps of:

providing a structure comprising a SiGe layer disposed over a strained semiconductor layer;

oxidizing said SiGe layer to form a SiGe oxide in a first region but not in a second region of said structure;

removing said SiGe oxide;

forming a surface channel device in said first region and a buried channel device in said second region such that the strained semiconductor layer serves as the channel layer of each device.

23. A structure comprising:

a strained semiconductor layer;

a surface channel device; and

a buried channel device, wherein said surface and buried channel devices include a channel comprising said strained semiconductor layer.

1 24. The structure as claimed in claim 23, wherein said strained semiconductor layer
2 comprises Si.

1 25. The structure as claimed in claim 23, wherein said structure further includes a relaxed
2 semiconductor layer.

1 26. The structure as claimed in claim 25, wherein said relaxed semiconductor layer comprises
2 SiGe.

1 27. A circuit formed by interconnecting the buried channel device and the surface channel
2 device of claim 23.